PCB Layout and Design Considerations for CH7015/CH7016 SDTV/HDTV Output Device

1. Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7015/CH7016 SDTV/HDTV Output Device. Guidelines in component placement, power supply decoupling, grounding, and reference crystal placement and selection, input signal interface and video components for both SDTV and HDTV output are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures shown in this document are based on a schematic with a CH7015/CH7016 designed with Intel i830 system.

2. Component Placement

Components associated with the CH7015/CH7016 encoder should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1mF ceramic capacitor to each of the power supply pins as shown in Figure 1 and Figure 2 . These capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7015/CH7016 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7015/CH7016 should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7015/CH7016 ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See Table 1 for the Ground pins assignment.

2.1.2 Power Supply Pins

Separate digital (including the I/O supply voltage VDDV), PLL, and DAC power planes are recommended. See Table 1 for the Power supply pins assignment.

Table 1: Power Supply Pins Assignment

Pin#	# of pins	Type	Symbol	Description
5,16,33	3	Power	DVDD	Digital Supply Voltage (3.3V)
8,18,31,39	4	Power	DGND	Digital Ground
34	1	Power	AVDD	Analog Supply Voltage (3.3V)
37	1	Power	AGND	Analog Ground
41	1	Power	VDDV	I/O Supply Voltage (1.5V)
28	1	Power	VDD	DAC Supply Voltage (3.3V)
19,26	2	Power	GND	Ground

- **Digital, DAC and PLL Power Pins Decoupling and Connection**

Figure 1 shows the decoupling and connection for the DVDD, AVDD and VDD.

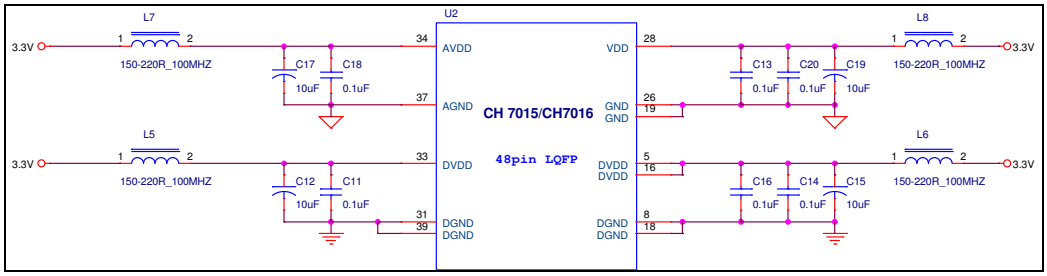


Figure 1: Digital, DAC and PLL Power Pins Decoupling and Connection

Note: All the Ferrite Beads described in this document are recommended to have <.05 W at DC; 2 3W at 25MHz & 47 W at 100MHz. Please refer to Fair_Rite part# 2743019447 for detail or an equivalent part can be used for the diagram.

- **VDDV and VREF Decoupling and Connection**

  VDDV is the I/O supply voltage (the amplitude of I/O signals varies from 0 to VDDV).

  VREF inputs a reference voltage of VDDV/2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, syncs and clock inputs. Please refer to **Figure 2** for the decoupling and connection.

  Figure 2 shows the decoupling and connection for the VDDV, VREF.

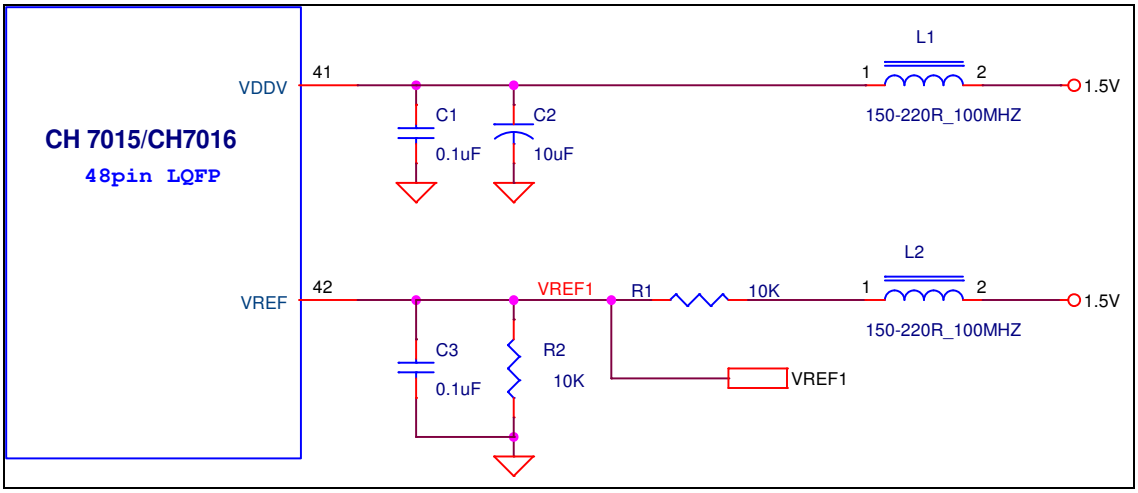


Figure 2: VDDV and VREF Decoupling and Connection

2.2 General Control

- **ISET Pin**

  A 147 Ω, 1% resistor should be placed directly and as close as possible to the ISET pin, (pin 24 - 44 pin pkg / pin 27 - 48 pin pkg.) , with short and wide traces, whenever possible. Otherwise, the ground reference of the ISET resistor should ideally be close to the CH7015/CH7016. See **Figure 3** for design reference.

- **GPIO [1: 0] Pins**

  These pins provide general purpose I/O and are controlled via the serial port. The direction of the signals is controlled by register 1Eh, GPIO Direction Control Register. When the direction is "input", the GPIO [1: 0] pins have a weak pull-up (about 1 MW), and can be used to discriminate the type of panel, the standard/type of TV, etc., during the system boot-up. See **Figure 3** for design reference. In the reference design, each GPIO pin is connected with a pair of resistors, which allow the designer to set it to either pull-up or pull-down. Using GPIO [0] (pin 14) as an example, if it should be set to HIGH, R1 can be 10 KW, and R3 should be not stuffed. If it is to be set to low, then R1 should be not stuffed, and R3 can be 10 KW.

- **RESET* Pin**

  RESET* pin, which is internal pull-up, When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port. In the reference design, the pin is connected to RST* of Intel's DVO control.

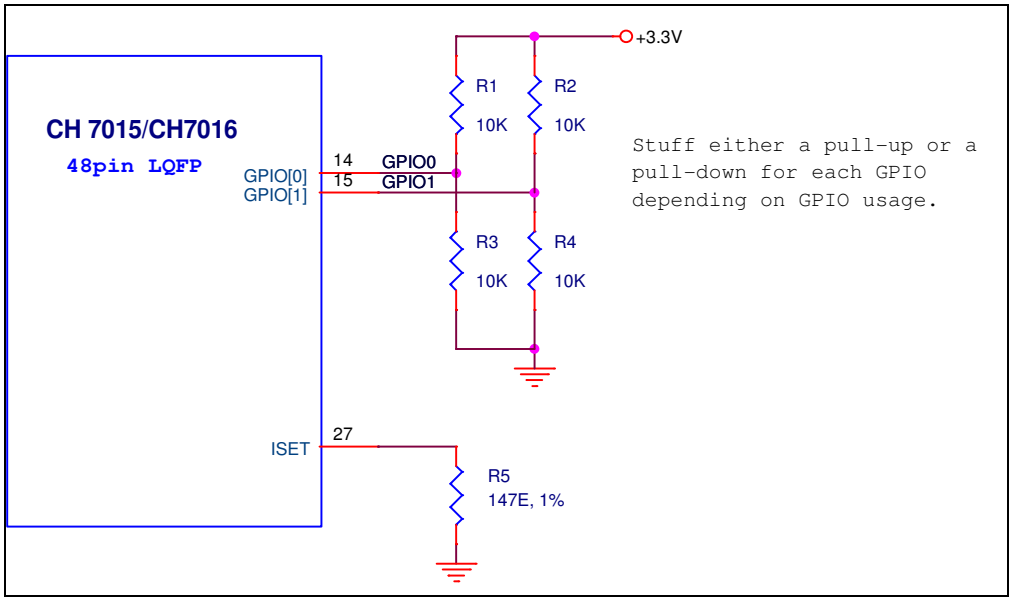


Figure 3: General Control Reference Design

2.3 Clock and Crystal Oscillator

- **XI/FIN and XO pins**

  Crystal Input

  The 14.31818 MHz (20ppm) crystal must be placed as close as possible to the XI/FIN and XO pins, (pin 32 & pin 33 - 44 pin pkg / pin 35 & pin 36 - 48 pin pkg.), with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7015/CH7016 encoder, it is very important that noise should not couple into these input pins. Traces with fast edge rates should not be routed under or adjacent these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected very close to the ground.

Reference Crystal Oscillator

The CH7015/CH7016 includes an oscillator circuit which allows an inexpensive 14.31818MHz crystal to be connected directly. Alternatively, an externally generated 14.31818MHz clock source may be supplied to the CH7015/CH7016. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI/FIN pin, and the XO pin should be left open. The external source must exhibit +/-20ppm or better frequency tolerance, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

Crystal is specified as 14.31818 MHz, +/-20 ppm fundamental type and in parallel resonance (NOT series resonance). Crystal is operated with a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to the CH7015/CH7016 (C_{ext}).

To allow tunability, a variable cap may be connected from XI/FIN to ground.

Note that the XI/FIN and XO pins each have approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI/FIN and XO pins, the following calculation should be used:

$$\mathbf{C_{ext} = (2 \times C_L) - C_{int} - 2C_S}$$

where:

C_{ext}= external load capacitance required on XI/FIN and XO pins.

C_L= crystal load capacitance specified by crystal manufacturer.

C_{int}= capacitance internal to CH7015/CH7016 (approximately 10-15 pF on each of XI/FIN and XO pins).

C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

Please refer to **Figure 4** for the symbols used in the calculation described above.

In general, let us assume

C_{int} XI/FIN = C_{int} XO = C_{int}

C_{ext} XI/FIN = C_{ext} XO = C_{ext}

such that

$C_L = (C_{int} + C\,ext) / 2 + C_S$ and $C\,ext = 2\,(C_L - C_S) - C_{int} = 2\,C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int}/2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in excessive drive level specified by crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For the detail consideration of crystal oscillator design, please refer AN-06.

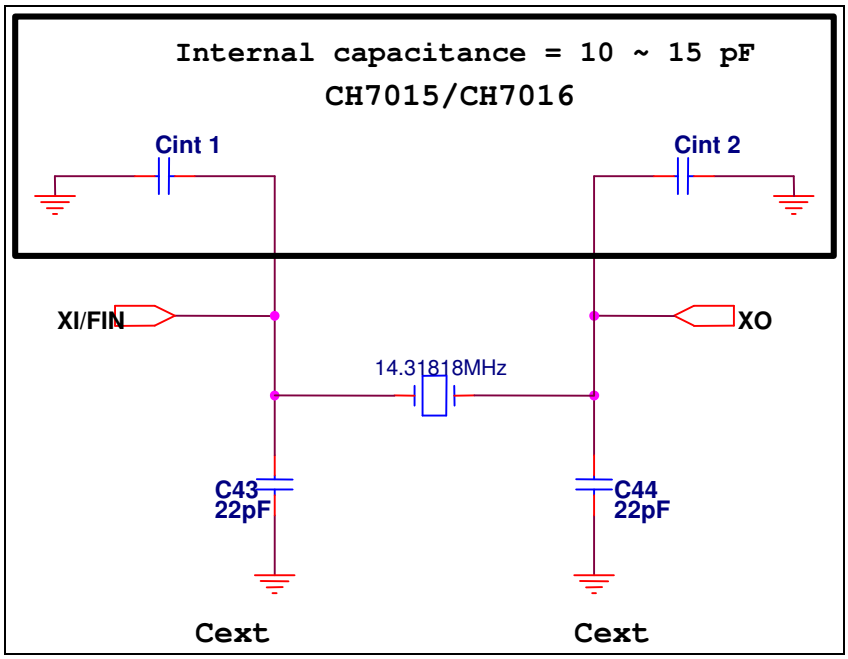


Figure 4: Reference Crystal Design.

- **P-Out pin**

  This pin provides a pixel clock signal to the VGA controller which can be used as a reference frequency. The output driver is driven from the VDDV supply (pin 38 - 44 pin pkg / pin41 - 48 pin pkg). In the reference design, this pin is connected to DVOBC_CLKIN (DVO clock input). This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.

- **XCLK, XCLK*(External Clocks Input) pins**

  XCLK and XCLK* form a differential clock signal input to CH7015/CH7016 for use with the H, V and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. In the reference design they are connected to DVOB_CLK and DVOB_CLK# (see **Figure 5** for reference design).

- **BCO (Buffered Clock Output) pin**

  The BCO pin (pin 35 - 44 pin pkg / pin 38 - 48 pin pkg.) provides buffered crystal oscillator clock output or VSYNC output in RGB bypass mode. This pin is driven by the DVDD supply. When it is used as a buffered clock out, the BCO register (register 22h) controls the types of the output clocks (see CH7015/CH7016 datasheet for details). It is very useful for troubleshooting. See TB-37 for the methods of measuring crystal clock and color burst frequencies using BCO pin.

  For the reference design of the clock pins, please see **Figure 5**.

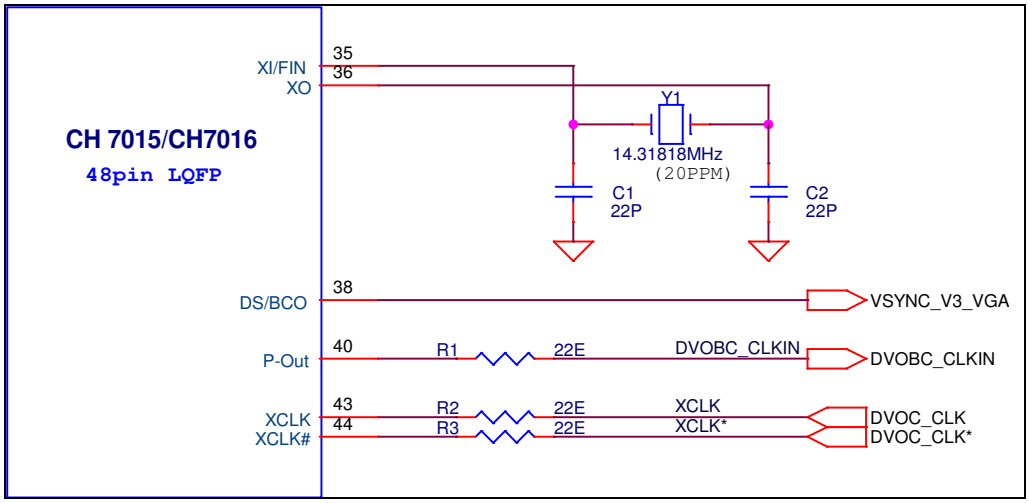


Figure 5: Clock and Crystal Oscillator Reference Design

2.4 Serial Ports Control

- **SPD and SPC pins**

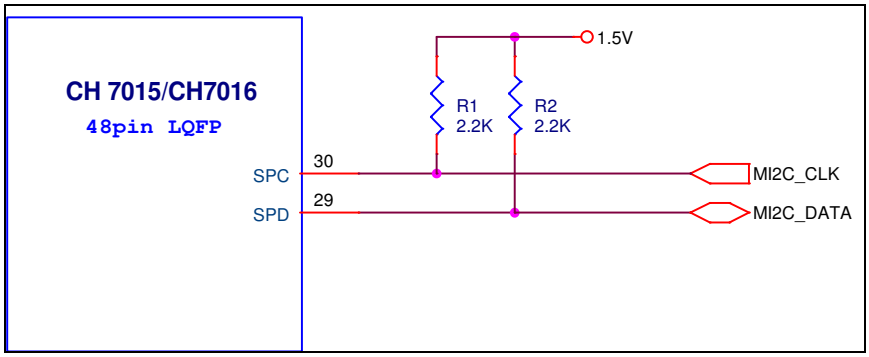


Figure 6: Serial Port Control Reference Design

2.5 Data Input and Syncs

Since the digital pixel data and the pixel clock of the CH7015/CH7016 may toggle at speeds up to 165MHz (depending on the input mode), it is critical that the connection of these video input signals between the graphics controller and the CH7015/CH7016 be kept short and isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals.

- **D[11:0]**

Each set of data pins accept a set of 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF is the threshold level. The two sets of data pins can be ganged together as a single 12 bits data port. The DATA signals are single ended high speed signals that should be routed together as a bus. It is recommended that 8 mil traces be used in routing these signals.

- **H and V**

  When the SYO control bit is low, these pins accept a horizontal/vertical sync inputs for use with the D[11:0] input data. The amplitude will be 0 to VDDV. VREF is the threshold level for these inputs.

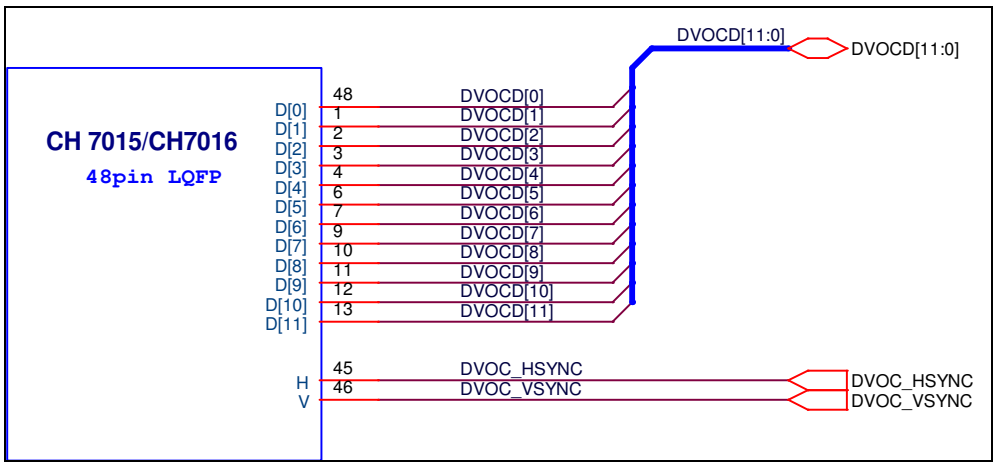


Figure 7: Data Input and Syncs Reference Design

2.6 TV Output and Control

In TV Output mode, multiplexed input data, sync and clock signals are input to the CH7015/CH7016 from the graphics controller 扭 digital output port. A P-OUT clock can be output as a frequency reference to the graphics controller, which is recommended to ensure accurate frequency generation. Horizontal and vertical sync signals are normally sent to the CH7015/CH7016 from the graphics controller, but can be output to the graphics controller as an option (this is not recommended for pixel rates above 50MHz). Data will be 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. The input data will be encoded into the selected video standard, and output from the video DACs. **Figure 8** shows the design example for TV out.

The components associated with the video output pins should be placed as close as possible to the CH7015/CH7016. The 75 W output termination, the output filter network, and the output connectors should be located as close as possible to the CH7015/CH7016 to minimize the noise pickup as well as possible reflections due to impedance mismatches. The video output signals should overlay the ground plane and should be routed away from digital lines that could introduce crosstalk. The Y and C outputs or Y, Pr and Pb signals should be separated by a ground trace and inductors and ferrite beads in series with these outputs should not be located next to each other.

The recommended output reconstruction filter network is a third order low pass filter. The recommended circuit elements for a typical S-Video and composite outputs are shown in **Figure 8**, and its corresponding frequency response is shown in **Figure 9** and **10**.

Table 2 shows the TV output configurations from the DACs.

48 pin LQFP		2 RCA + 1 S-Video	SCART	
CVBS/B	(pin 21)	CVBS	CVBS	
Y/G	(pin 25)	Y	G	
C/R	(pin 23)	C	R	
CVBS	(pin 17)	CVBS	B	
		VGA-Bypass RGB	**HDTV**	**SDTV**
Pb/B	(pin 23)	B	Pb	Pb
Y/G	(pin 24)	G	Y	Y
Pb/R	(pin 22)	R	Pr	Pr
CVBS	(pin 17)			CVBS

Table 2 TV Output Configurations

If the application calls for CVBS/S-video, SCART, RGB and YPrPb to output on one set of DAC output pins, different reconstruction filters for each type of signals can be implemented on the break-out cables. **Figure 11** shows the connection for the SCART output.

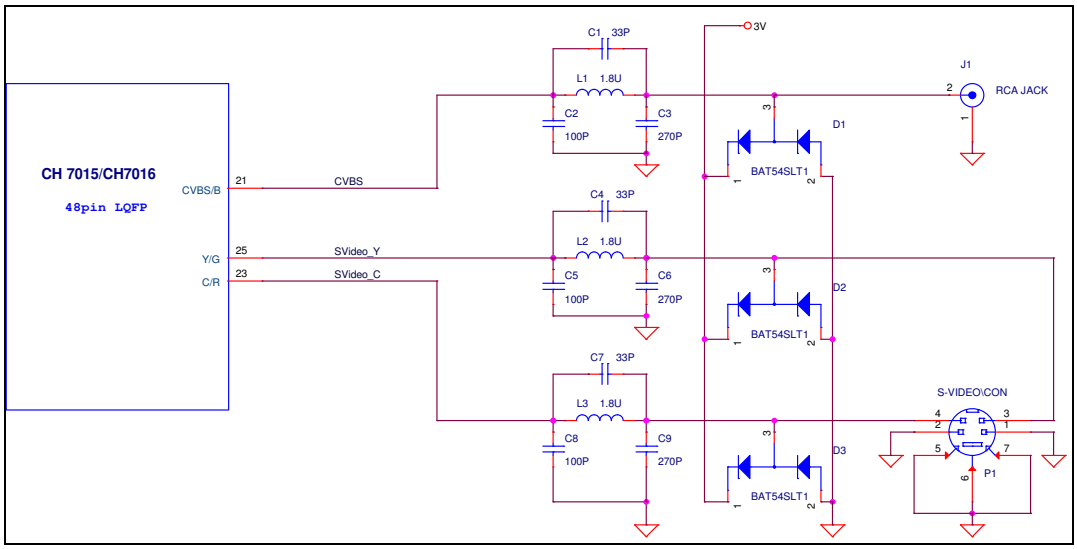


Figure 8: The Typical Connection For the S-Video and Composite Outputs

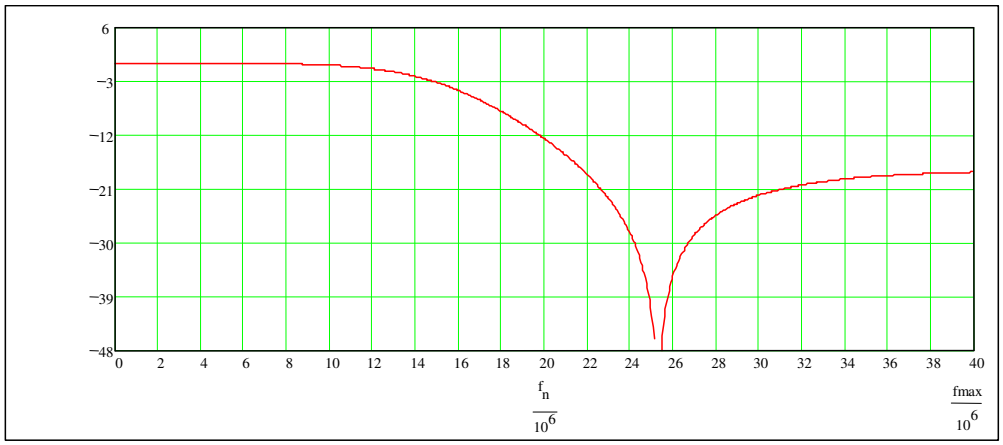


Figure 9: Amplitude Response of the 3rd Order Reconstruction Filter

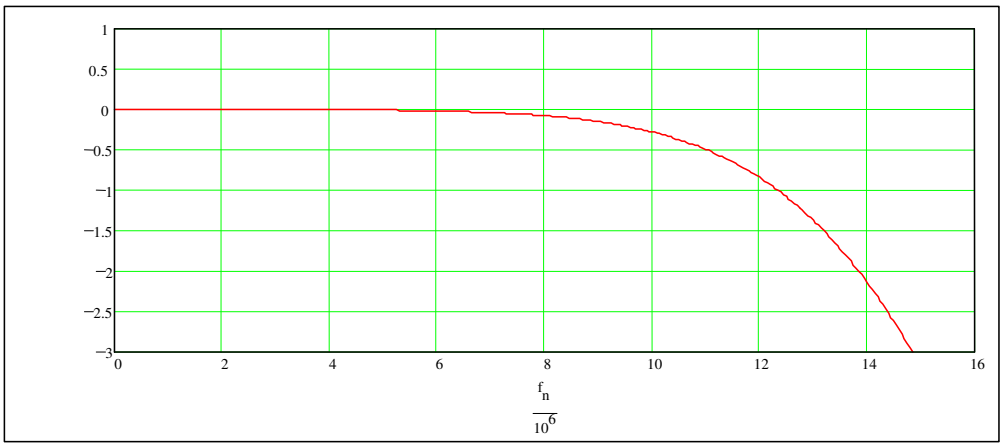


Figure 10: The Details of the Amplitude Response of the Pass Band

Note: If the application only allows one video output connection and simultaneously display of S-Video and Composite is not needed, please refer AN-46 on how to achieve the desired configuration.

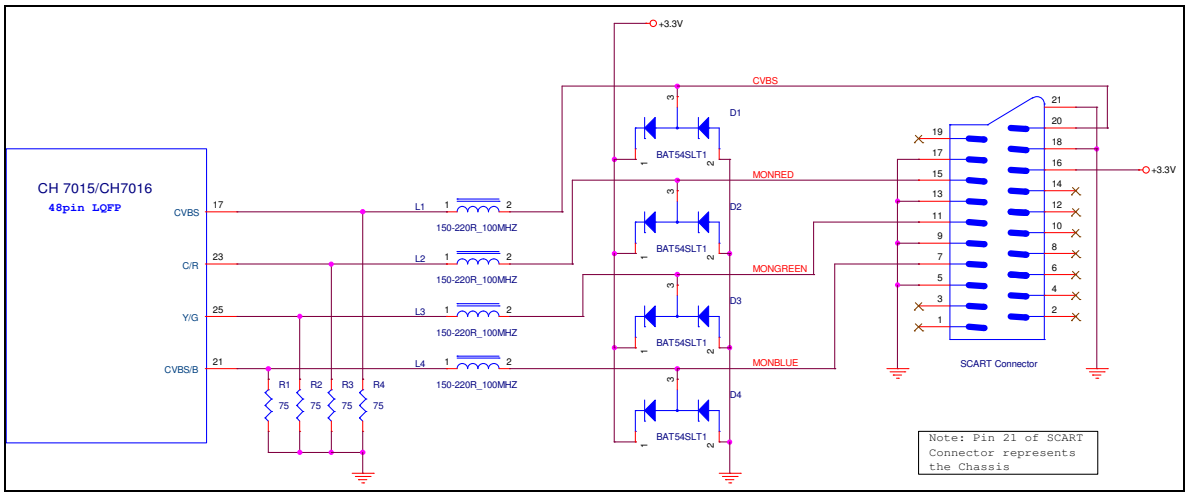


Figure 11: The connection for the SCART connector

Careful layout consideration for the CVBS, Y and C (or CVBS, R, G and B) traces and the attached components are needed in order to avoid the signal coupling among each other. It is suggested that the signal traces of Y, C and CVBS be separated with the ground traces and routed to the connectors. Also, the capacitors and the inductors attached to those outputs should not be placed too close to each other.

2.7 HDTV Output and Control

In HDTV mode, data, sync and clock signals are input to the CH7015/CH7016 from a graphics device in the scanning method that matches the display device (interlaced data is sent to the CH7015/CH7016 to drive an interlaced display, non-interlaced data is sent to the CH7015/CH7016 to drive a non interlaced display). The input data format can be YCrCb or RGB. A clock signal (P-Out) can be output as a frequency reference to the graphics device. Horizontal and vertical sync signals must either be sent to the CH7015/CH7016 from the graphics device or embedded in the data stream according to SMPTE standards. Data is 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. Input data is color space converted to the selected video format, has sync signals generated and is output from the video DAC 扭. The output format is YPrPb. No scaling, scan conversion or flicker filtering is applied in HDTV Bypass mode.

Careful layout consideration for the Y, Pr, Pb traces and the attached components are needed in order to avoid the signal coupling among each other. It is suggested that the signal traces of Y, Pr, Pb be separated with the ground traces and routed to the connectors. Also, the capacitors and the inductors attached to those outputs should not be placed too close to each other.

2.8 HDTV and SDTV Reconstruction Filters

Different reconstruction filters are to be used for the YPrPb component output signals depending on the resolution or Y, Pr, Pb type. If HDTV (480p, 576p, 720p, 1080i) is desired, then the circuit as described in **Figure 12** should be used. Alternatively, if SDTV (480i, 576i) is desired, then the circuit from **Figure 13** should be followed. For the Y/G DAC in **Figure 12**, the reconstruction filter comprises of capacitors C13, C12, and C17 and the inductor L6.

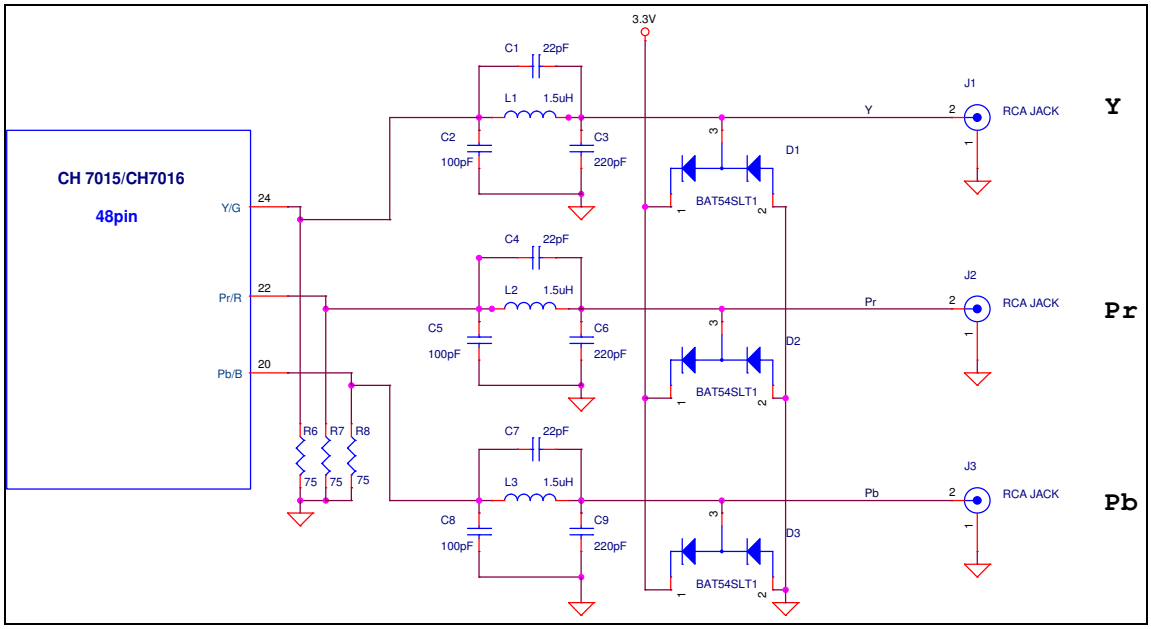


Figure 12: Reconstruction filter and connection for HDTV/YPrPb output

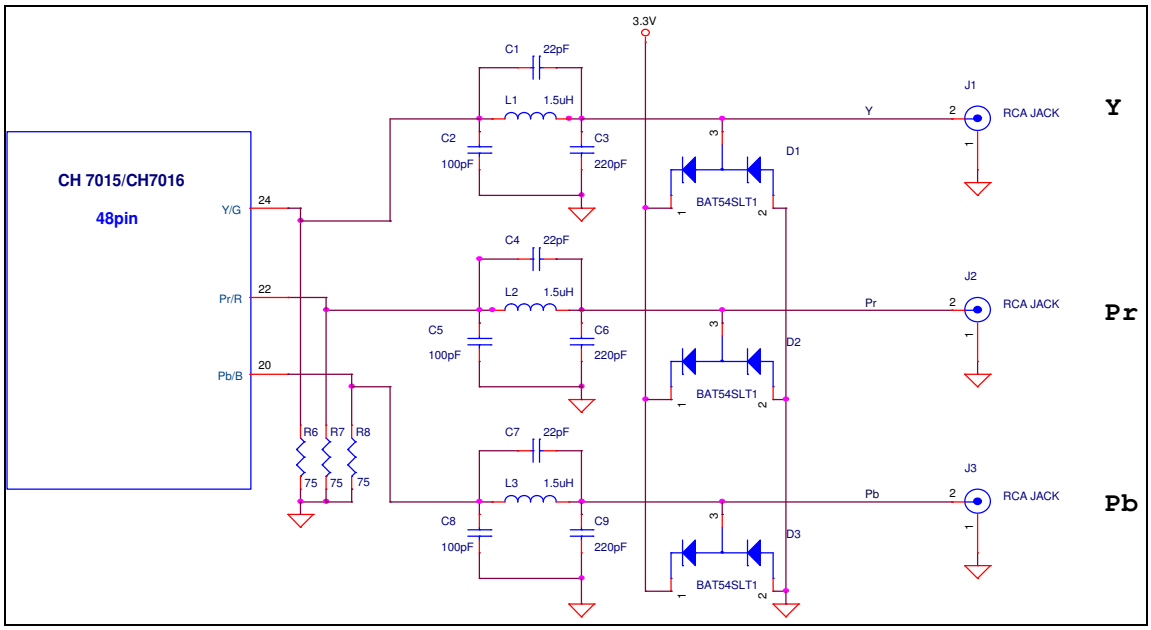
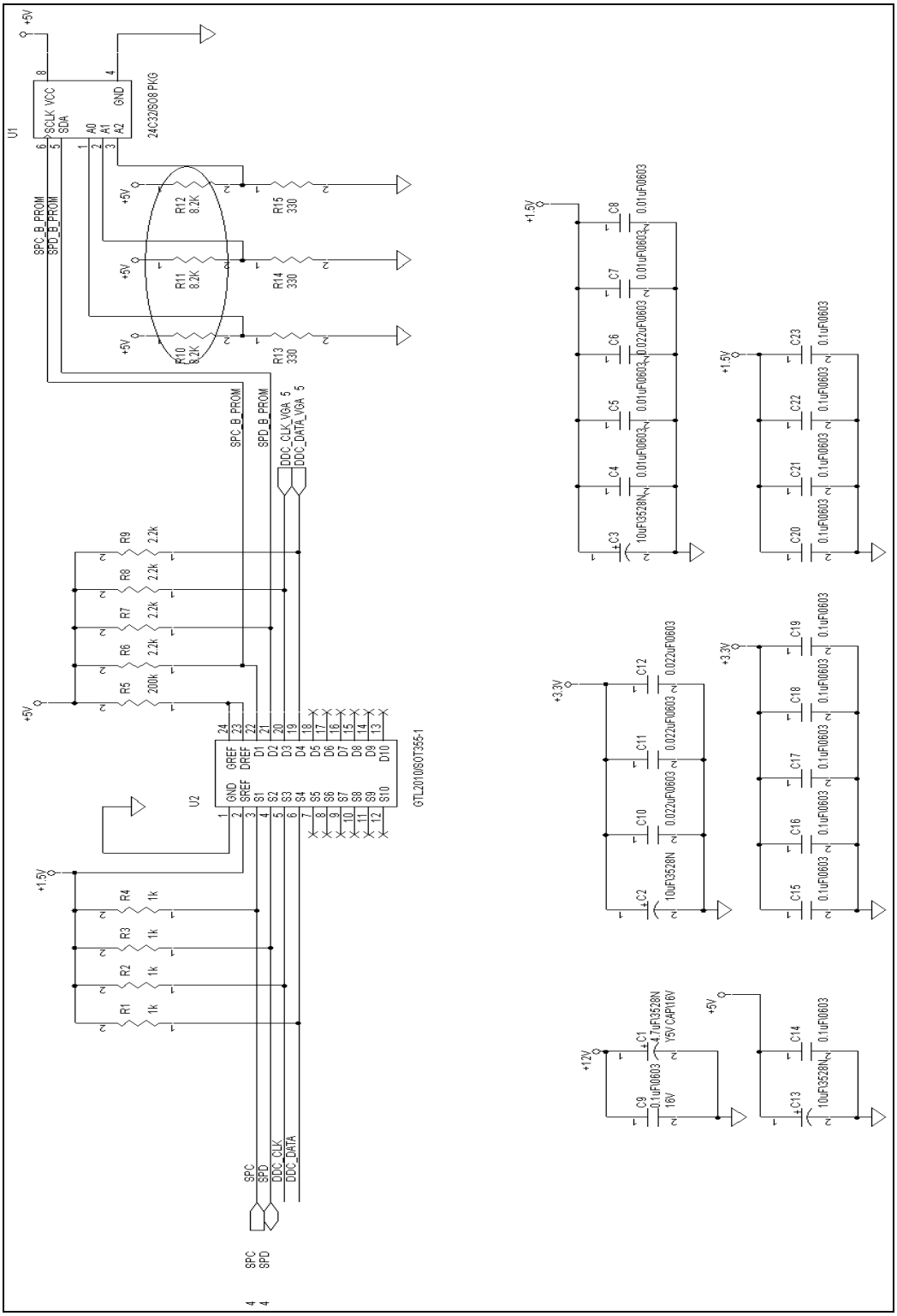
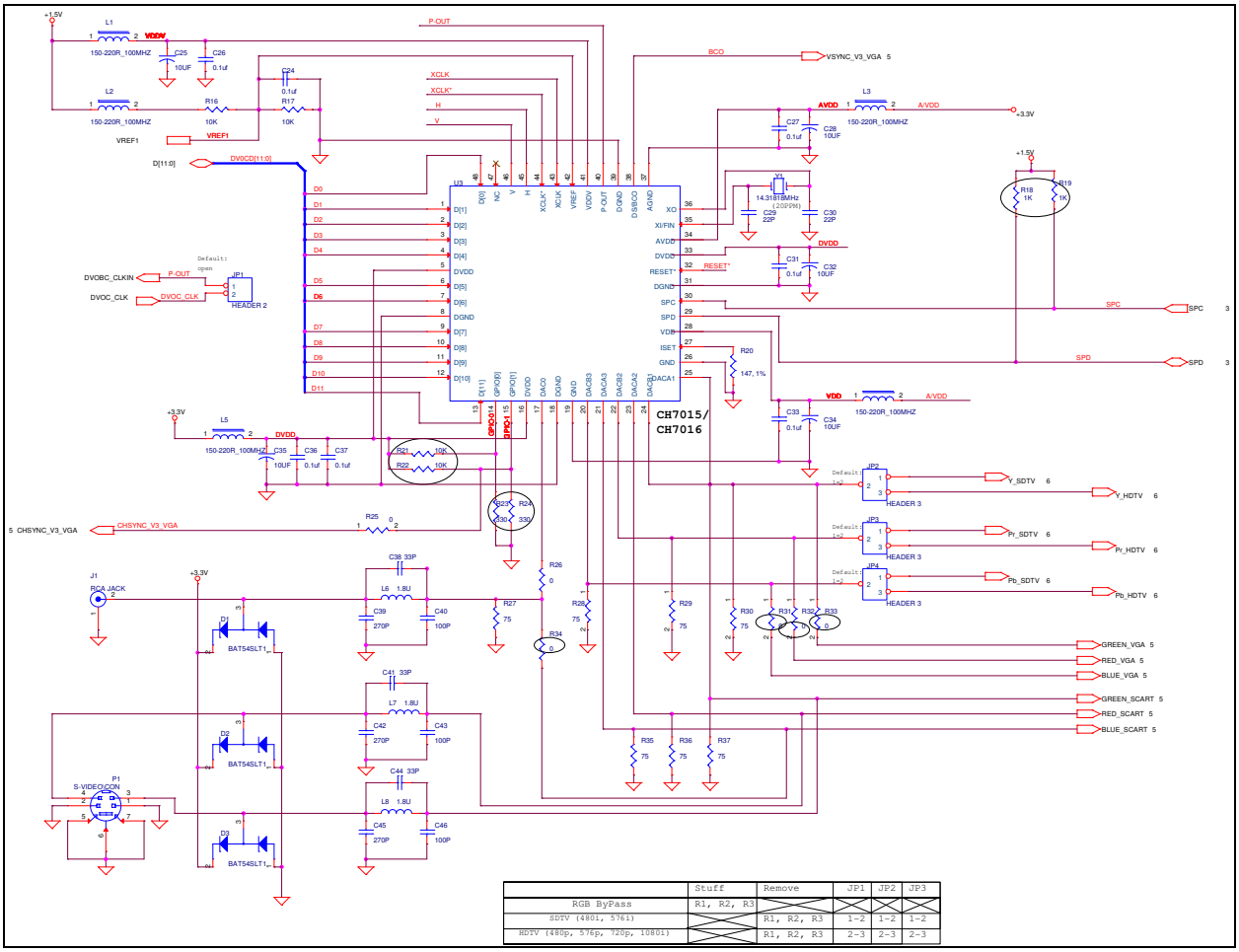


Figure 13: Reconstruction filter and connection for SDTV/YPrPb output

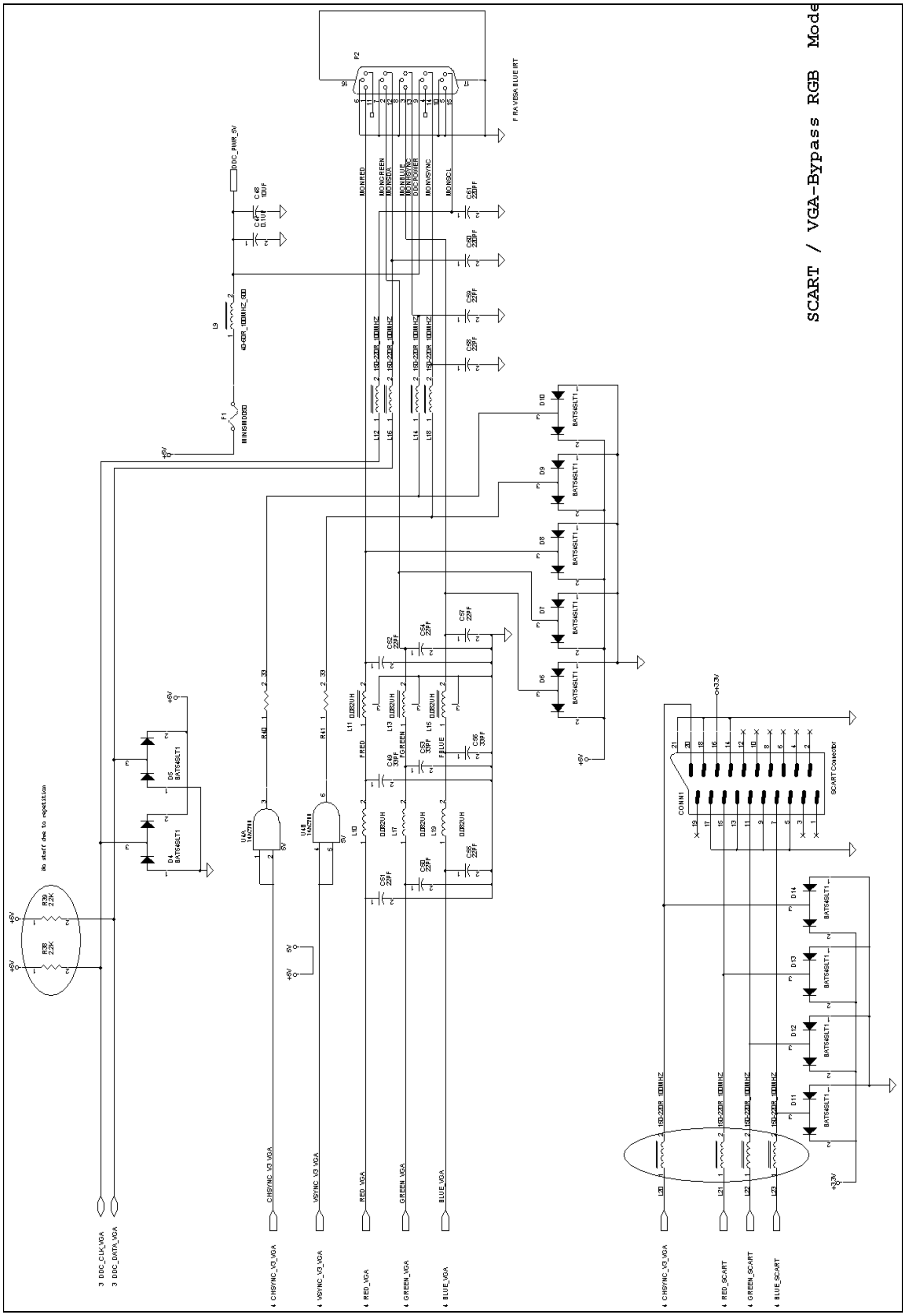
3. Reference Design Example

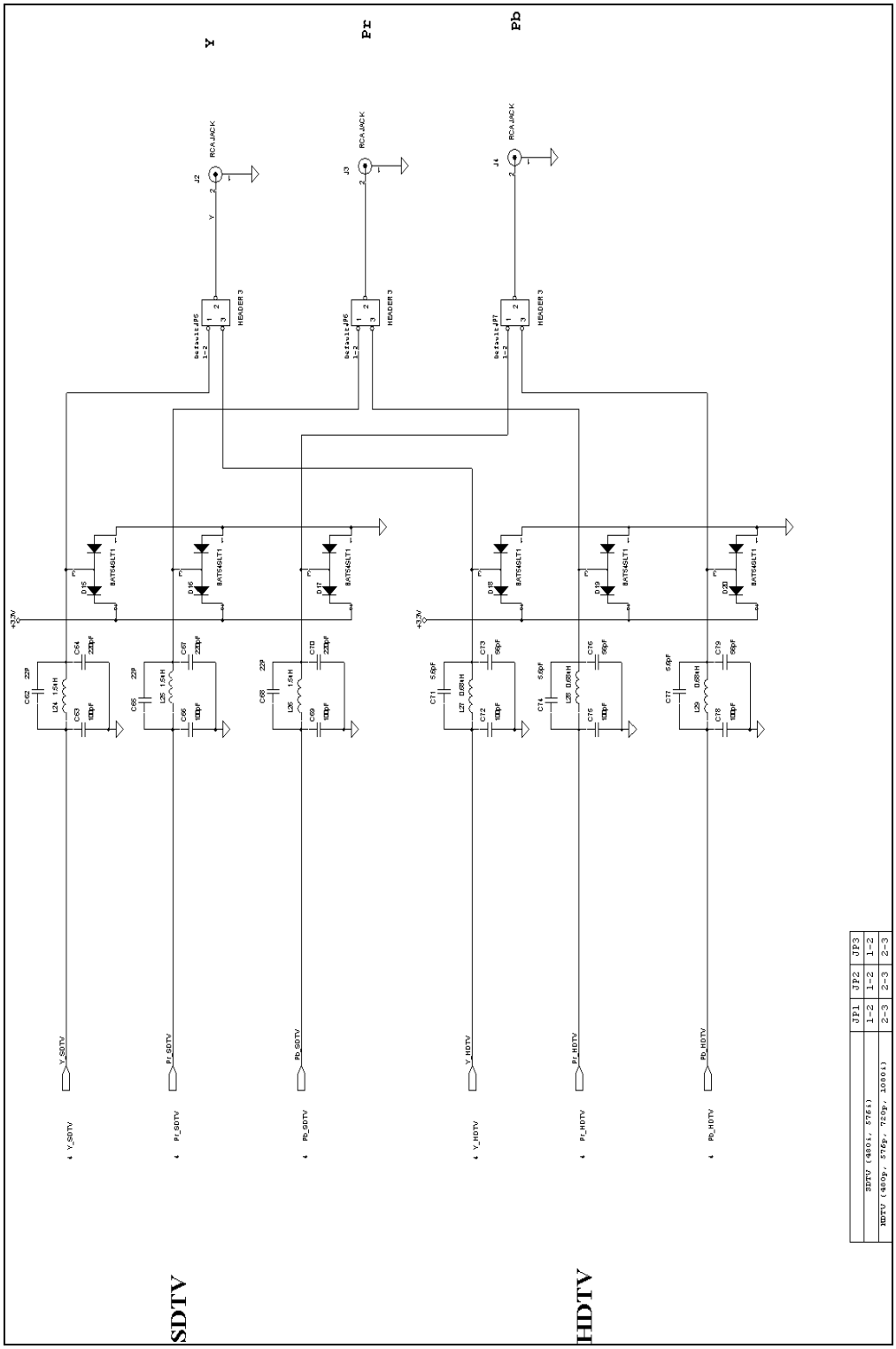
The following schematic is for CH7015/CH7016 PCB design example only. It is not a complete design. Those who are seriously doing and application design with CH7015/CH7016 and would like to have a complete reference schematic design should contact Applications within Chrontel, Inc.


U1
24C32BS08 PKG
SCLK VCC
SDA
GND
A0
A1
A2
SPC_B_PROM
SPD_B_PROM
+5V
R12 8.2K
R11 8.2K
R10 8.2K
R15 330
R14 330
R13 330
DDC_CLK_VGA 5
DDC_DATA_VGA 5
R9 2.2k
R8 2.2k
R7 2.2k
R6 2.2k
R5 200k
U2
GTL2010SOT353-1
GND
SREF
GREF
DREF
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
+1.5V
R4 1k
R3 1k
R2 1k
R1 1k
SPC
SPD
DDC_CLK
DDC_DATA
C8 0.01uF0603
C7 0.01uF0603
C6 0.022uF0603
C5 0.01uF0603
C4 0.01uF0603
C3 10uF3528N
C23 0.1uF0603
C22 0.1uF0603
C21 0.1uF0603
C20 0.1uF0603
+3.3V
C12 0.022uF0603
C11 0.022uF0603
C10 0.022uF0603
C2 10uF3528N
C19 0.1uF0603
C18 0.1uF0603
C17 0.1uF0603
C16 0.1uF0603
C15 0.1uF0603
+12V
C1 4.7uF3528N
Y5V CAP/16V
C9 0.01uF0603
16V
C14 0.1uF0603
C13 10uF3528N



	Stuff	Remove	JP1	JP2	JP3
RGB ByPass	R1, R2, R3				
SDTV (480i, 576i)		R1, R2, R3	1-2	1-2	1-2
HDTV (480p, 576p, 720p, 1080i)		R1, R2, R3	2-3	2-3	2-3


SCART / VGA-Bypass RGB Mode


Y
Pr
Pb
SDTV
HDTV
RCA JACK
HEADER 3
BAT54SLT1
+3.3V
Y_SDTV
Pr_SDTV
Pb_SDTV
Y_HDTV
Pr_HDTV
Pb_HDTV
JP1 JP2 JP3
1-2 1-2 1-2
2-3 2-3 2-3
SDTV (480i, 576i)
HDTV (480p, 576p, 720p, 1080i)

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